In the Claims:

Claims 1 -20 (canceled)

Claim 21 (new): A method for forming a field-effect transistor on a substrate, said method comprising:

forming a high-k dielectric layer over said substrate;

forming a gate electrode layer over said high-k dielectric layer;

etching said gate electrode layer and said high-k dielectric layer to form a gate stack comprising a high-k dielectric segment situated over said substrate and a gate electrode segment situated over said high-k dielectric segment, said step of etching said gate electrode layer and said high-k dielectric layer being performed in a plasma process chamber;

performing a nitridation process in said plasma process chamber on said gate stack, said nitridation process utilizing a nitrogen containing plasma to nitridate sidewalls of said high-k dielectric segment, said nitridation process on said high-k dielectric segment causing nitrogen to enter said high-k dielectric segment, said nitrogen forming an oxygen diffusion barrier in said high-k dielectric segment and preventing lateral diffusion of oxygen into said high-k dielectric segment;

repairing damage on said sidewalls of said high-k dielectric segment caused during said step of etching said gate electrode layer and said high-k dielectric layer.

Claim 22 (new): The method of claim 21 wherein said high-k dielectric layer comprises hafnium oxide.

Claim 23 (new): The method of claim 21 wherein said high-k dielectric layer comprises hafnium silicate.

Claim 24 (new): The method of claim 21 wherein said high-k dielectric layer comprises zirconium oxide.

Claim 25 (new): The method of claim 21 wherein said high-k dielectric layer comprises zirconium silicate.

Claim 26 (new): The method of claim 21 wherein said high-k dielectric layer comprises aluminum oxide.

Claim 27 (new): The method of claim 21 wherein said gate electrode segment comprises polysilicon.

Claim 28 (new): A method for forming a field-effect transistor including a high-k dielectric layer situated over a substrate and a gate electrode layer situated over said high-k dielectric layer, said method comprising steps of:

etching said gate electrode layer and said high-k dielectric layer to form a gate stack, said gate stack comprising a high-k dielectric segment situated over said substrate and a gate electrode segment situated over said high-k dielectric segment, said gate stack comprising sidewalls;

utilizing a nitrogen plasma to nitridate said sidewalls of said gate stack;

wherein said step of etching said gate electrode layer and said high-k dielectric layer to form said gate stack is performed in a plasma process chamber being utilized to perform said step of performing said nitridation process on said gate stack;

repairing damage on said sidewalls of said gate stack caused during said step of etching said gate electrode layer and said high-k dielectric layer;

forming source/drain regions adjacent to said gate stack;

fabricating spacers on said sidewalls of said gate stack;

performing a rapid thermal anneal on said gate stack.

Claim 29 (new): The method of claim 28 wherein said high-k dielectric layer comprises hafnium oxide.

Claim 30 (new): The method of claim 28 wherein said high-k dielectric layer comprises hafnium silicate.

Claim 31 (new): The method of claim 28 wherein said high-k dielectric layer comprises zirconium oxide.

Claim 32 (new): The method of claim 28 wherein said high-k dielectric layer comprises zirconium silicate.

Claim 33 (new): The method of claim 28 wherein said high-k dielectric layer comprises aluminum oxide.

Claim 34 (new): The method of claim 28 wherein said gate electrode segment comprises polysilicon.